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Question 1 Part (a)



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Question 1 Part (b)



Question 1 Part (c)

 

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Question 1 Part (d)



A correction circuit is needed for the switch-tail ring counter to ensure that there is never a zero between two of the ones because if this should happen (it could happen on power-up) without a correction circuit it would be unable to correct (i.e. the zero would circulate indefinitely).

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2. (a) 1st Row: input change : 01 to 11 input change: 01 to 00

 

 2nd Row: input change : 00 to 01 input change: 00 to 10

 

 3rd Row: input change: 11 to 01 input change: 10 to 00

 

 4th Row: input change: 11 to 01 input change: 10 to 00

 

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2. (b)

 

 Expanded Flow Table

 

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2. (c)



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3. (a) 

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3.(b)



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3. (c) & (d)



Output map can be impoved by realizing the 2 ‘don’t care’ situations

 

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3. (e)

 S-R latch implementation

 

Complement functions for NAND latches



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Question 3 (e)

Logic Diagram



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4 (a)



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4. (b)



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4.(c)

The minimum change in the analog volatge that will cause a change in the least significant bit of the digitally converted number OR



OR the voltage difference between two consecutive numbers of the binary conversion

(d)

The number of analog to digital conversions per unit time OR possibly

 Increasing the sample rate results in more binary numbers that must be stored in the file but leads to better quality ausio or video.

(e)



The time between the ‘start conversion’ and the ‘data valid’ is the time required for the ADC to convert the analog voltage to a digital number.